

IN THE CLAIMS:

Please amend claims 1, 4, 5, 8, 9, 11 and 15, and cancel claims 2, 3, 6, 14 and 18 as follows:

1           1. (currently amended) A method for processing tasks in a data  
2 processing system including a microprocessor and an instruction cache  
3 wherein tasks of various types are defined in the system, each task type  
4 having code associated therewith, the tasks being processed ~~out of~~  
5 ~~sequential order~~ by loading the associated code into the instruction cache  
6 for execution on the microprocessor, the method comprising: ~~the step of~~  
7           placing tasks of same task type into a batch such that the tasks in  
8 a batch are processed before processing ~~the~~ a next ordered task; ~~and~~  
9           if the code associated with at least one type of task fits  
10 within the instruction cache, processing such a task by loading the  
11 associated code into the instruction cache and executing the code on  
12 the microprocessor, and, on a determination that there is a further  
13 task of like type in the batch, executing the loaded code to process  
14 the further task;  
15           if the code associated with at least one type of task is not capable  
16 of being loaded as a whole into the instruction cache, logically dividing  
17 the code at one or more break points into two or more portions, and  
18 wherein during processing of such a task, responding to a break point  
19 defined within a first portion of the code to schedule a further task for  
20 future execution of a second portion of the code;  
21           wherein the tasks of the same task type use same code in the  
22 instruction cache; and  
23           wherein the tasks are placed in the batch at the time the tasks are  
24 scheduled.

2. (cancelled)

3. (cancelled)

1           4. (currently amended) A method as claimed in claim 3 1  
2 wherein the further scheduled task is placed in a batch of like  
3 tasks.

1           5. (currently amended) A method as claimed in claim 3 1  
2 wherein each of portions of code defines an atomic operation.

6. (cancelled)

1           7. (previously presented) A method as claimed in claim 1  
2 wherein the tasks are managed as a queue.

1           8. (currently amended) A computer program product comprising a  
2 computer ~~usable~~ readable medium having computer readable program code  
3 ~~means~~ embodied in the medium for processing tasks in a data  
4 processing system, the data processing system including a  
5 microprocessor and an instruction cache and wherein tasks of various  
6 types are defined in the system, each task type having code  
7 associated therewith, the tasks being processed ~~out of sequential~~  
8 ~~order~~ by executing the associated code on the microprocessor, the  
9 program code ~~means~~ comprising code ~~means~~ for:

10           scheduling tasks of same type into a batch such that tasks in a  
11 batch are processed before processing ~~the~~ a next ordered task,  
12 wherein the tasks of the same type use the same program code;

13           if the code associated with at least one type of task fits  
14 within the instruction cache, processing such a task by loading the  
15 associated code into the instruction cache and executing the code on  
16 the microprocessor, and, on a determination that there is a further  
17 task of like type in the batch, executing the loaded code to process  
18 the further task;

19           if the code associated with at least one type of task is not  
20 capable of being loaded as a whole into the instruction cache,  
21 logically dividing the code at one or more break points into two or  
22 more portions, and wherein during processing of such a task,  
23 responding to a break point defined within a first portion of the  
24 code to schedule a further task for future execution of a second  
25 portion of the code;

26           wherein the tasks of the same task type use same code in the  
27 instruction cache; and

28           wherein the tasks are placed in the batch at the time the tasks  
29 are scheduled.

1           9. (currently amended) Data processing ~~apparatus~~ system comprising  
2 a microprocessor and an instruction cache wherein tasks of various types  
3 are defined in the system, each task type having code associated  
4 therewith, the ~~apparatus including~~ system comprising:

5           means for processing the tasks ~~out of sequential order~~ by loading  
6 the associated code into the instruction cache for execution on the  
7 microprocessor; and

8           if the code associated with at least one type of task fits  
9 within the instruction cache, means for processing such a task by  
10 loading the associated code into the instruction cache and executing  
11 the code on the microprocessor, and, on a determination that there is  
12 a further task of like type in the batch, executing the loaded code  
13 to process the further task;

14           if the code associated with at least one type of task is not capable  
15 of being loaded as a whole into the instruction cache, means for logically  
16 dividing the code at one or more break points into two or more portions,  
17 and wherein during processing of such a task, responding to a break point  
18 defined within a first portion of the code to schedule a further task for  
19 future execution of a second portion of the code;

20           means for scheduling tasks of same type into a batch, wherein the  
21 means for processing the tasks is operable to process the tasks in a batch  
22 before processing ~~the~~ a next ordered task; and

23           wherein the tasks of the same type use the same program code; and  
24           wherein the tasks are placed in the batch at the time the tasks are  
25 scheduled.

1           10. (original) Data processing apparatus as claimed in claim 9  
2 wherein the microprocessor and ~~i-cache~~ instruction cache are embodied on a  
3 single chip.

1           11. (currently amended) A computerized method for scheduling tasks  
2 in a task queue, the method comprising:

3           identifying a new task to be scheduled in the task queue;

4           determining if the task queue includes a cached task that requires  
5 ~~the~~ a same code to process the cached task and the new task; and

6           batching the new task with the cached task if the task queue  
7 includes the cached task that requires the same code to process the cached

task and the new task;

if the code associated with at least one type of task fits within the instruction cache, processing such a task by loading the associated code into the instruction cache and executing the code on the microprocessor, and, on a determination that there is a further task of like type in the batch, executing the loaded code to process the further task;

if the code associated with at least one type of task is not capable of being loaded as a whole into the instruction cache, logically dividing the code at one or more break points into two or more portions, and wherein during processing of such a task, responding to a break point defined within a first portion of the code to schedule a further task for future execution of a second portion of the code; and

wherein the tasks are placed in the batch at the time the tasks are scheduled.

12. (previously presented) The method of claim 11, further comprising adding the new task to the end of the queue if the task queue does not include the cached task that requires the same code to process the cached task as the new task.

13. (previously presented) The method of claim 11, further comprising:  
loading task code for processing the cached task into an instruction cache;  
executing the task code for processing the cached task in the instruction cache; and  
executing the task code for processing the new task in the instruction cache without loading new code into the instruction cache.

14. (cancelled)

15. (currently amended) A computer program product embodied in a tangible computer readable media for processing tasks in a data processing system comprising:

~~computer readable program codes coupled to the tangible media for~~  
scheduling tasks in a task queue, the ~~computer readable~~ program codes

6 comprising codes configured to cause the program to:

7       identify a new task to be scheduled in the task queue;

8       determine if the task queue includes a cached task that requires the  
9 same code to process the cached task and the new task; ~~and~~

10       batch the new task with the cached task if the task queue includes  
11 the cached task that requires the same code to process the cached task and  
12 the new task;

13       if the code associated with at least one type of task fits  
14 within the instruction cache, process such a task by loading the  
15 associated code into the instruction cache and execute the code on  
16 the microprocessor, and, on a determination that there is a further  
17 task of like type in the batch, execute the loaded code to process  
18 the further task;

19       if the code associated with at least one type of task is not capable  
20 of being loaded as a whole into the instruction cache, logically dividing  
21 the code at one or more break points into two or more portions, and  
22 wherein during processing of such a task, respond to a break point defined  
23 within a first portion of the code to schedule a further task for future  
24 execution of a second portion of the code; and

25       wherein the tasks are placed in the batch at the time the tasks are  
26 scheduled.

1       16. (previously presented) The computer program product of claim  
2 15, wherein the program code is further configured ~~to cause the program to~~  
3 add the new task to the end of the queue if the task queue does not  
4 include the cached task that requires the same code to process the cached  
5 task as the new task.

1       17. (previously presented) The computer program product of claim  
2 15, wherein the program code is further configured ~~to cause the program~~  
3 to:

4       load task code for processing the cached task into an instruction  
5 cache;

6       execute the task code for processing the cached task in the  
7 instruction cache; and

8           execute the task code for processing the new task in the instruction  
9   cache without loading new code into the instruction cache.

18. (cancelled)